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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,933	LIN, MING-REN	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

In view of the arguments presented in the Appeal Brief filed September 15th, 2003, paper No. 19, prosecution on the merits is reopened to address the issues raised in the Brief. The grounds of rejections in the prior Office actions are withdrawn, and new grounds of rejection are presented here. 37 CFR 1.193 (b)(2) applies:

(2) Where prosecution is reopened by the primary examiner after an appeal or reply brief has been filed, appellant must exercise one of the following two options to avoid abandonment of the application:

(i) File a reply under § 1.111, if the Office action is not final, or a reply under § 1.113, if the Office action is final; or

(ii) Request reinstatement of the appeal. If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (§ § 1.130, 1.131 or 1.132) or other evidence are permitted.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori et al. (U.S. Patent 6,252,294) in view of Yamaguchi et al. (U.S. Patent 6,271,541).

In re claim 1, Hattori discloses a method of manufacturing a semiconductor device on a silicon-on-insulator wafer (col. 4, lines 32-45) including a silicon active layer

(FIG. 2: 4) having at least two die pads (FIG. 1: 1a) formed thereon, the at least two die pads separated by at least one scribe lane (FIG. 1: 1b), comprising the steps of (col. 4, line 8 to col. 6, line 47 and FIGS. 1-5D): forming at least one cavity (FIGS. 2 and 3A-C: 6) through the silicon active layer (FIG. 2: 4) and the buried oxide layer (FIG. 2: 3) in the at least one scribe lane (FIG. 2) ; forming at least one gettering plug (FIGS. 2 and 3A-C: 7) in each cavity, each gettering plug comprising a polycrystalline silicon formed by CVD deposition (col. 5, line 66 to col. 6, line 5) containing a plurality of gettering sites; and subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites (col. 4, line 41 to col. 5, line 10 and FIGS. 1-5D);

Hattori does not explicitly disclose wherein each gettering plug comprising doped fill material containing a plurality of gettering sites as recited in present independent claim 1.

Yamaguchi discloses a method of manufacturing a semiconductor device on a silicon-on-insulator wafer (FIG. 1: 1) (col. 7, lines 45-58) including a silicon active layer (FIG. 1: 12), comprising the steps of (col. 7, line 38 to col. 8, line 42 and FIGS. 1-8): forming at least one cavity (FIG. 1) through the silicon active layer and the buried oxide layer (FIG. 1: 4) (col. 6, lines 47-60); forming at least one gettering plug (FIG. 1: 13 and 15) in each cavity (col. 6, line 61 to col. 7, line 5), each gettering plug comprising a doped polysilicon material (col. 8, lines 32-42) containing a plurality of gettering sites; and subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites (col. 8, lines 33-38 and FIGS. 1-8). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of

Hattori and Yamaguchi to enable the gettering plug comprising doped fill material of Hattori to be formed and furthermore to remove the heavy metal impurity by gettering (col. 7, lines 4-5). Additionally, the gettering capability of the doped polysicion plug can be added to that of the polysilicon regions 19 and 20. This permits a further increase in the gettering capability of the overall device (col. 8, lines 39-42).

In re claim 2, Yamaguchi discloses wherein the doped fill material is polysilicon formed by deposition of the polysilicon and a dopant in the cavity (col. 8, lines 36-42). Additionally, Tseng (U.S. Patent 5,677,222) discloses that the doped fill material is polysilicon (FIG. 15: 232) formed by LPCVD deposition of the polysilicon and the dopant in the cavity (FIG. 15: 231), the doped polysilicon is doped using P^{31} (col. 5, line 63 to col. 6, line 2). Thus, Tseng provides evidence that the process of forming a doped fill material by LPCVD deposition of the polysilicon and a dopant in the cavity is well-known to one of ordinary skill in the art of making semiconductor devices.

In re claims 3 and 4, it is well-known to one of ordinary skill in the art of making semiconductor devices that the dopant might be one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon, and germanium.

In re claim 5, Hattori discloses wherein the steps of forming at least one cavity further comprises forming a sidewall liner in the cavity (col. 8, lines 54-57 and FIGS. 1-5).

In re claim 6, Hattori discloses wherein the gettering plug (FIG. 2: 7) extends down through the silicon active layer (FIG. 2: 4), and contacts a dielectric insulation layer (FIG. 2: 3) on the wafer.

In re claim 7, Hattori discloses wherein the gettering plug (FIGS. 3A-C: 7) extends down through both a silicon active layer (FIGS. 3A-C: 4) and a dielectric insulation layer (FIGS. 3A-C: 3) on the wafer.

In re claim 8, Hattori discloses wherein the gettering step gettered impurities migrate into the silicon substrate layer below the dielectric insulation layer (col. 4, lines 41-51).

2. Claims 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori et al. (U.S. Patent 6,252,294) in view of Yamaguchi et al. (U.S. Patent 6,271,541).

In re claim 9, Hattori discloses a method of gettering impurities on a silicon-on-insulator wafer (col. 4, lines 32-45) including a silicon active layer (FIG. 2: 4) having at least two die pads formed thereon, the at least two die pads (FIG. 1: 1a) separated by at least one scribe lane (FIG. 1: 1b), comprising the steps of (col. 4, line 8 to col. 6, line 47 and FIGS. 1-5D): forming at least one cavity (FIGS. 2 and 3A-C: 6) through the silicon active layer (FIG. 2: 4) in the at least one scribe lane (FIG. 2) ; filling the cavity with a fill material (2: 7) to form at least one gettering plug (FIGS. 2 and 3A-C: 7) including a plurality of gettering sites; and subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites (col. 4, line 41 to col. 5, line 10 and FIGS. 1-5D);

Hattori does not explicitly disclose adding at least one dopant to the fill material to form at least one gettering plug including a plurality of gettering sites as recited in present independent claim 9.

Yamaguchi discloses a method of manufacturing a semiconductor device on a silicon-on-insulator wafer (FIG. 1: 1) (col. 7, lines 45-58) including a silicon active layer (FIG. 1: 12), comprising the steps of (col. 7, line 38 to col. 8, line 42 and FIGS. 1-8): forming at least one cavity (FIG. 1) through the silicon active layer and the buried oxide layer (FIG. 1: 4) (col. 6, lines 47-60); forming at least one gettering plug (FIG. 1: 13 and 15) in each cavity (col. 6, line 61 to col. 7, line 5), each gettering plug comprising a doped polysilicon material (col. 8, lines 32-42) containing a plurality of gettering sites; and subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites (col. 8, lines 33-38 and FIGS. 1-8). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Hattori and Yamaguchi to enable the gettering plug comprising doped fill material of Hattori to be formed and furthermore to remove the heavy metal impurity by gettering (col. 7, lines 4-5). Additionally, the gettering capability of the doped polysilicon plug can be added to that of the polysilicon regions 19 and 20. This permits a further increase in the gettering capability of the overall device (col. 8, lines 39-42).

In re claim 10, it is well-known to one of ordinary skill in the art of making semiconductor devices that the dopant may be one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon, and germanium.

In re claim 11, Hattori discloses wherein the steps of forming at least one cavity further comprises forming a sidewall liner in the cavity (col. 8, lines 54-57 and FIGS. 1-5).

In re claim 12, Yamaguchi discloses wherein the fill material is polysilicon, and the dopant is added by one of codeposition and implantation (col. 8, lines 32-42).

In re claim 13, Hattori discloses wherein the gettering plug (FIG. 2: 7) extends through the silicon active layer (FIG. 2: 4), and contacts a dielectric insulation layer (FIG. 2: 3) on the wafer.

In re claim 14, Hattori discloses wherein the gettering plug (FIGS. 3A-C: 7) extends through both the silicon active layer (FIGS. 3A-C: 4) and a dielectric insulation layer (FIGS. 3A-C: 3) on the wafer.

In re claim 15, Hattori discloses wherein the gettering step gettered impurities migrate into the silicon substrate layer below the dielectric insulation layer (col. 4, lines 41-51).

3. Claims 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori et al. (U.S. Patent 6,252,294) in view of Yamaguchi et al. (U.S. Patent 6,271,541).

In re claim 21, Hattori discloses a method of gettering impurities on a silicon-on-insulator wafer (col. 4, lines 32-45) including a silicon active layer (FIG. 2: 4), buried oxide layer (FIG. 2: 3) and a silicon substrate (FIG. 2: 2), the silicon active layer having at least two die pads (FIG. 1: 1a) formed thereon, the at least two die pads separated by at least one scribe lane (FIG. 1: 1b), comprising the steps of (col. 4, line 8 to col. 6, line 47 and FIGS. 1-5D): forming a plurality of cavities (FIGS. 2 and 3A-C: 6) through the

silicon active layer (FIGS. 2 and 3A-C: 4) and the buried oxide layer (FIGS. 2 and 3A-C: 3) to the silicon substrate (FIGS. 2 and 3A-C: 2) in the at least one scribe lane (FIG. 2) ; filling the cavities with a fill material (2: 7) to form at least one gettering plug (FIGS. 2 and 3A-C: 7) including a plurality of gettering sites; and subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites (col. 4, line 41 to col. 5, line 10 and FIGS. 1-5D);

Hattori does not explicitly disclose implanting at least one dopant into the fill material in the cavities to form at least one gettering plug including a plurality of gettering sites as recited in present independent claim 21.

Yamaguchi discloses a method of manufacturing a semiconductor device on a silicon-on-insulator wafer (FIG. 1: 1) (col. 7, lines 45-58) including a silicon active layer (FIG. 1: 12), comprising the steps of (col. 7, line 38 to col. 8, line 42 and FIGS. 1-8): forming at least one cavity (FIG. 1) through the silicon active layer and the buried oxide layer (FIG. 1: 4) (col. 6, lines 47-60); forming at least one gettering plug (FIG. 1: 13 and 15) in each cavity (col. 6, line 61 to col. 7, line 5), each gettering plug comprising a doped polysilicon material (col. 8, lines 32-42) containing a plurality of gettering sites; and subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites (col. 8, lines 33-38 and FIGS. 1-8). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Hattori and Yamaguchi to enable the gettering plug comprising doped fill material of Hattori to be formed and furthermore to remove the heavy metal impurity by gettering (col. 7, lines 4-5). Additionally, the gettering capability of the doped polysilicon plug can

be added to that of the polysilicon regions 19 and 20. This permits a further increase in the gettering capability of the overall device (col. 8, lines 39-42).

In re claim 22, Hattori discloses wherein the gettering step, gettered impurities move into the silicon substrate (col. 4, lines 41-51).

In re claim 23, Hattori discloses wherein the wafer comprises a plurality of adjacent die pads (FIG. 1: 1a) and a single scribe lane (FIG. 1: 1b) separated each die pad from the adjacent die pads (FIG. 1).

In re claim 24, Hattori discloses wherein the scribe lane comprises a single row of gettering plugs, a pair of parallel rows of gettering plugs (FIG. 2: 7) or a pair of parallel gettering trenches (FIGS. 1-2).

In re claim 25, it is well-known to one of ordinary skill in the art of making semiconductor devices that the dopant may be one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon, and germanium.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
April 19, 2004

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800